A-6

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/985,971	11/07/2001	Wen-Yen Lin	MR2663-30	4610

4586 7590 09/03/2003

ROSENBERG, KLEIN & LEE
3458 ELLICOTT CENTER DRIVE-SUITE 101
ELLICOTT CITY, MD 21043

EXAMINER
GLENN, KIMBERLY E

ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 09/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/985,971	LIN ET AL.	
	Examiner	Art Unit	
	Kimberly E Glenn	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 June 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-5 and 7-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *4* is/are allowed.

6)☒ Claim(s) *1,5 and 7-14* is/are rejected.

7)☒ Claim(s) *3* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by Wojnarowski et al US Patent 5,108,825. (Of record)

Wojnarowski et al disclose a high density interconnect structure (printed circuit board) comprising a plurality of electronic chips 15 disposed in the cavity of a substrate 12, a dielectric layer 20 covers the electronic chip as well as the substrate. Each chip has a plurality of electronic contact pads 16 disposed on the upper surface. These contact pads 16 are used to make external electrical connection between the individual chips. The dielectric layer 20 is had plurality of vias disposed over the plurality of contact pads. A layer of metallization 32 is disposed over the dielectric layer, which extend into the vias 25 to make electrical contact between selected contact pads. Alternatively, dielectric layers 40 60 and 80 and metallization layers 50 70 and 90 overlap the first metallization layer. The method step to the above disclosed apparatus are inherent. The dielectric layer 20 is comprised of Kapton polyimide layer, which has a high dielectric constant. With regards to the metallization layer, Wojnarowski et al refers reader to previous disclosed patents. Wojnarowski et al discloses a patent, US Patent 4,783,695, by C. W. Eichelberger titled "Multichip Integrated Circuit Packaging Configuration and Method". Eichelberger et al '695 disclose a method of fabricating a high density interconnect structure. Eichelberger et al '695 discloses in column 10 line 41 that the metallization layers are

copper. (See figure 1 and column 5, line 21-38, column 7, line 18 through column 9, line 60 and column 12, lines 30-41)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 7-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wojnarowski et al US Patent 5,108,825 in view of Pluymer et al US Patent 5,945,897.

The primary reference, Wojnarowski et al teaches a high density interconnect structure (printed circuit board) comprising a plurality of electronic chips 15 disposed in the cavity of a substrate 12, a dielectric layer 20 covers the electronic chip as well as the substrate. Each chip has a plurality of electronic contact pads 16 disposed on the upper surface. These contact pads 16 are used to make external electrical connection between the individual chips. The dielectric layer 20 is had plurality of vias disposed over the plurality of contact pads. A layer of

metallization 32 is disposed over the dielectric layer, which extend into the vias 25 to make electrical contact between selected contact pads. Alternatively, dielectric layers 40 60 and 80and metallization layers 50 70 and 90 on disposed on the first metallization layer. The method step to the above disclosed apparatus are inherent. The dielectric layer 20 is comprised of Kapton polyimide layer, which has a high dielectric constant. With regards to the metallization layer, Wojnarowski et al refers reader to previous disclosed patents. Wojnarowski et al discloses a patent, US Patent 4,783,695, by C. W. Eichelberger titled "Multichip Integrated Circuit Packaging Configuration and Method". Eichelberger et al '695 disclose a method of fabricating a high density interconnect structure. Eichelberger et al '695 discloses in column 10, lines 41 that the metallization layer are copper. (See figure 1 and column 5, line 21-38, column 7, line 18 through column 9, line 60 and column 12, lines 30-41)

Thus, Wojnarowski et al is shown to teach all the limitation of the claim with the exception of a metallic ground layer mounted on a first side of the dielectric substrate.

Pluymers et al disclose in prior art figure 1, a HDI module with a ground layer 20. (See figure 1)

One skilled in the art, at the time of the invention, would have found it obvious to provide the HDI interconnect structure of Wojnarowski et al with a ground layer as taught by Pluymers et al. The motivation / suggestion for this modification would be to provide a heat and dc return for the chips.

Response to Arguments

Applicant's arguments filed 6/17/03 have been fully considered but they are not persuasive. Applicant argues that the Wojnarowski et al reference does not teach a printed

circuit board. In response to applicants arguments, Wojnarowski et al teaches a high density interconnect structure (printed circuit board) comprising a plurality of electronic chips 15 (line layer) disposed in the cavity of a substrate 12, a dielectric layer 20(isolation layer) covers the electronic chip as well as the substrate. Each chip has a plurality of electronic contact pads 16 disposed on the upper surface. These contact pads 16 are used to make external electrical connection between the individual chips. The dielectric layer 20 is had plurality of vias disposed over the plurality of contact pads. A layer of metallization 32(highly conductive layer) is disposed over the dielectric layer, which extends into the vias 25 to make electrical contact between selected contact pads. (See column 4, lines 53-55, column 5, lines 27-32, column 12, lines 33-41 and column 13, line 50 through column 14 line 2)

Allowable Subject Matter

Claim 3 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 4 is allowed.

The following is a statement of reasons for the indication of allowable subject matter: The prior art of record does not disclose or fairly teach a determining a pre-estimated values of an effective dielectric constant, determining a shortened sized of a microwave circuit based on this pre-estimated value and making a printed circuit board containing the microwave circuit according to the shortened sized that is determined.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Mowatt et al US Patent 5,432,677 teaches a circuit module having a ground layer, Arledge et al US Patent 6,493,198 disclose a high density printed circuit board having a ground layer, and Dupont " Kapton Type and Thickness" 1996-1999 disclose the characteristic of Kapton.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimberly E Glenn whose telephone number is (703) 306-5942. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on (703) 308-4909. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Kimberly E Glenn
Examiner
Art Unit 2817

keg

Robert Pascal
Supervisory Patent Examiner
Technology Center 2800